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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LOGSDON, JOSEPH B	
ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 01/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/090,096	CHUI ET AL.	
	Examiner	Art Unit	
	Joe Logsdon	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Objections:

1. The abstract of the disclosure is objected to because it is too long. The abstract should not exceed 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Rejections—35 U.S.C. 112, First Paragraph:

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-49 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. According to claims 1, 34, and 42, the fixed-length transmission unit size of the buffers comprises a software programmable parameter changeable by the user without the need to change existing hardware. The specification does not mention anywhere that the fixed-length transmission unit size of the buffers comprises a software programmable parameter changeable by the user without the need to change existing hardware. The specification only states that the cell size and word size are programmable (page 31, lines 10-12). Claims 2-33, 35-41, and 43-49 depend on claims 1, 34, and 42 and are therefore similarly rejected.

Claim Rejections—35 U.S.C. 103(a):

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-3, 22, 25-32, 42-45, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. in view of Parry.

With regard to claims 1, 3, 42, and 43, Takamichi et al. discloses an ATM cell rate supervising apparatus comprising at least one bidirectional FIFO unit, wherein each such bidirectional FIFO unit comprises a first and second unidirectional FIFO buffer (Fig. 6; column 6, lines 28-32; cell buffer pairs 51-55, 7-8, and 61-65). Takamichi et al. fails to disclose an invention for which the buffer word size is programmable. Parry teaches a FIFO buffer that is

useful for ATM applications and whose word size can be programmed by either using more that one FIFO or varying the width of the input data bus (Fig. 3; column 13, lines 23-39). Because the word size can be programmed, the cell size can be programmed (see the specification at page 30, line 27 to page 31, line 3). It would have been obvious to one of ordinary skill in the art to modify the invention of Takamichi et al. so that the word size of each of the FIFO buffers is programmable, as in Parry, because such a modification allows the invention to be used on a larger number of servers because servers vary in the word size they handle. Neither Takamichi et al. nor Parry teaches that the fixed-length transmission unit size of the buffers comprises a software programmable parameter changeable by the user without the need to change existing hardware. Examiner takes Official Notice that it has been well known in the art that any portion of an input data bus, wherein the portion has a width less than or equal to the width of the data bus, can be used without in any manner modifying the input data bus itself. It would have been obvious to one of ordinary skill in the art to modify the invention of Takamichi et al. so that the fixed-length transmission unit size of the buffers comprises a software programmable parameter changeable by the user without the need to change existing hardware because Examiner takes Official Notice that it has been well known in the art that any portion of an input data bus, wherein the portion has a width less than or equal to the width of the data bus, can be used without in any manner modifying the input data bus itself, and, therefore, the fixed-length transmission unit size of the buffers could be changed without changing existing hardware, which would allow the invention to be used, without modification of existing hardware, on a larger number of servers because servers vary in the word size they handle.

With regard to claims 2, 26, 28, 44, and 45, Takamichi et al. fails to address the issue of the timing of the read and write ports. Parry teaches that in a synchronous FIFO separate read and write clocks are used for the read and write ports, respectively (column 1, lines 54-57; column 5, lines 53-64; column 6, lines 44-55). Because they use separate clocks, the read and write ports are asynchronous with respect to each other. It would have been obvious to one of ordinary skill in the art to design the system of Takamichi et al. so that the read and write ports use read and write clocks, and that the read and write clocks are asynchronous with each other, as in Parry, so that activities within the switching platform can be coordinated and so that the switch can perform two non-interfering activities, such as reading from one buffer and writing to the other buffer, simultaneously and at different rates.

With regard to claims 22, 25, and 48, Takamichi et al. fails to disclose an invention for which each unidirectional buffer outputs a signal that indicates space available for at least one more cell in the unidirectional FIFO buffer or for which each unidirectional buffer outputs a signal that indicates that at least one cell is in the unidirectional FIFO buffer. Parry teaches a FIFO that uses "empty" and "full" flags (abstract; column 2, lines 59-68). A "full" flag is used when it is not the case that space is available for at least one more cell in the unidirectional buffer, and an "empty" flag is used when it is not the case that there is at least one cell in the unidirectional buffer. It would have been obvious to one of ordinary skill in the art to modify the invention of Takamichi et al. so that it uses "empty" and "full" flags, as in Parry, because such an arrangement prevents unsuccessful read and write operations.

With regard to claims 27, 29, and 30, the limitations that the write clock operates at about 50 megahertz, or that the read clock operates at about 21 or 42 megahertz are obvious design

choices. The choice of operating frequency depends in part on the frequencies the devices used by the system can handle.

With regard to claim 31, Takamichi et al. fails to teach that the contents of the buffers can be modified. Parry teaches a data switching system and method for which data may be selectively modified in the buffers ("memory devices"; column 3, lines 1-23). Parry teaches that modification of the buffer contents is particularly useful for ATM to take advantage of any CRC code present in the cell (column 2, lines 40-46). It would have been obvious to one of ordinary skill in the art to modify the invention of Takamichi et al. so that the contents of the buffers can be modified, as in Parry, because such an arrangement would provide an efficient strategy for error detection and/or correction.

With regard to claim 32, it would have been obvious to one of ordinary skill in the art that the inclusion of two switches is a design choice; switches of different kinds can be interconnected as needed.

7. Claims 4-18 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. and Parry as applied to claims 1 and 42 above, and further in view of Kou et al. Both Takamichi et al. and Parry teach that their inventions are useful for ATM networks. In particular, Takamichi et al. teaches that the output of the first FIFO buffer (buffer 65 in Fig. 6) goes to an ATM switch (3 in Fig. 1) (column 6, lines 28-32) and the input of the second buffer (buffer 61 in Fig. 6) comes from the same ATM switch. Neither Takamichi et al. nor Parry teach that their inventions could be interfaced with ATM, frame relay, voice, data, T1, E1, T3, E3, OC3, and OC12, or that their inventions could be interfaced with sources of varying bandwidths.

Kou et al. teaches an ATM switching system, in which the switch implements an output-buffer type cell-based switching architecture that supports interfaces to ATM OC3/DS3/DS1, SMDS DS3/DS1, and Frame Relay DS1 (see e.g., the abstract and the discussion of Figure 1). In section 7, Kou et al. points out that the ATM backbone will migrate to OC12. An ATM switch can therefore serve as an interface between ATM and frame relay, voice, or data, as well as sources of varying bandwidths such as the bandwidths that are characteristic of T1, E1, T3, E3, OC3, and OC12. It would have been obvious to one of ordinary skill in the art that the inventions of Takamichi et al. and Parry could have been modified so that either the buffers transfer cells between the above listed interfaces; or the buffers transfer cells to and from switches that are connected to one of the above listed interfaces; or the buffers transfer cells to and from switches that can be designed to route cells to an OC12 trunk line; or the buffers transfer cells to and from service modules (which can themselves comprise interfaces) which use T1, E1, T3, E3, OC3, or OC12. It would further have been obvious to one of ordinary skill in the art that using such interfaces is advantageous because it allows the invention to offer more service types to more customers.

8. Claims 19 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. and Parry as applied to claims 1 and 42, respectively, and further in view of Morgan. Both Takamichi et al. and Parry fail to teach a diagnostic interface that supports a non-destructive read from the bidirectional FIFO unit while at least one cell is being written to and read from the bidirectional FIFO unit. Morgan teaches a circuit that enables the output buffer when data contained in the output buffer is valid. The fact that this circuit, which is a diagnostic

interface, performs a nondestructive read on the data is inherent to the invention because the memory device disclosed in Morgan transmits data only after it has been read and found to be valid. It would have been obvious to one of ordinary skill in the art to modify the inventions of Takamichi et al. and Parry so that they employ a diagnostic interface that supports a nondestructive read of the bidirectional buffer because such an arrangement helps to ensure that only valid data will be transmitted.

9. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. and Parry as applied to claim 1, and further in view of Morgan. Neither Takamichi et al. nor Parry discloses an apparatus in which a cell bus controller is coupled to a service module, a master bidirectional FIFO buffer is contained within the cell bus controller, a slave bidirectional FIFO buffer is contained within the service module, and the cell bus controller is connected to a switch. Morgan teaches a system that drives stored data onto a bidirectional bus, where the system comprises a cell bus controller ("initiating means"); a service module ("output means"), which is connected to the cell bus controller; and a master memory device ("memory") coupled to the cell bus controller (claim 1). It would have been obvious to one of ordinary skill in the art that the apparatus disclosed in Morgan could be easily modified so that the master memory device is contained within the cell bus controller because the master memory device in Morgan is coupled to the cell bus controller. The fact that a slave memory device is contained within the service module is inherent to the invention of Morgan because the service module ("output means") is capable of temporarily storing data (claim 1, column 13, lines 56-60). It would have been obvious to one of ordinary skill in the art to modify the inventions disclosed in Takamichi

et al. and Parry so that a cell bus controller is coupled to a service module, a master bidirectional FIFO buffer is contained within the cell bus controller, a slave bidirectional FIFO buffer is contained within the service module, and the cell bus controller is connected to a switch, consistent with the invention disclosed in Morgan, because, as taught by Morgan, such an arrangement allows data to be output only when it is valid (abstract).

10. Claims 20, 21, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. and Parry as applied to claims 1 and 42 above, and further in view of Christidou et al. Neither Takamichi et al. nor Parry discloses a bidirectional buffer for which each unidirectional buffer can send cells to the other unidirectional buffer for diagnostic purposes. Christidou et al. teaches a bidirectional queue in which the first unidirectional buffer sends a packet to the second unidirectional buffer with probability p_1, and the second unidirectional buffer sends a packet to the first unidirectional buffer with probability p_2. It would have been obvious to one of ordinary skill in the art that modifying the invention of Takamichi et al. or Parry so that the unidirectional buffers route cells to each other with nonzero probabilities, as in Christidou et al., and so that these probabilities can be set to 0 or 1 as desired would allow diagnostics to be performed on the switch platform; for example, if the delay of cells that traverse the first unidirectional buffer tends to be large, cells currently present in the first unidirectional buffer can be temporarily routed to the second unidirectional buffer in an attempt to find the source of the problem.

11. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. and Parry as applied to claim 22 above, and further in view of Caldara et al. Neither Takamichi et al. nor Parry discloses an invention in which a master bidirectional buffer is inhibited from reading to a slave bidirectional buffer based on feedback from the slave bidirectional buffer. Caldara et al. teaches an invention in which when slave buffers ("output buffers") become filled to a predetermined threshold level a feedback message is provided to the master buffers ("input buffers") to stop the reading ("transmission") of cells from the master buffers to the slave buffers (abstract; column 1, lines 38-50). It would have been obvious to one of ordinary skill in the art to modify the inventions disclosed by Takamichi et al. and Parry by Including this feedback because such feedback allows for effective flow control.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dockser and Wang et al. are cited to show the state of the art.

Response to Arguments:

13. Applicant argues that the combination of Takamichi et al. with Parry would not have been obvious to one of ordinary skill in the art. But consider what one of ordinary skill in the art might do, after finding the patent to Takamichi et al., to seek more information that may be useful to design a device similar to that taught in Takamichi et al. Takamichi et al. teaches at least two fifo buffers and an atm switch. One of ordinary skill in the art might then try the following expression for a text search:

first adj fifo with second adj fifo and atm adj switch with cell and fifo adj buffer

The result would be three U.S. Patents—one of which is the patent to Parry. So the two patents are indeed related.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Logsdon whose telephone number is (703) 305-2419. The examiner can normally be reached on Monday through Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached on (703) 305-4744.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4700.

15. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9314

For informal or draft communications, please label "PROPOSED" or "DRAFT".

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Joe Logsdon

Patent Examiner

Saturday, December 29, 2001

HASSAN KIZOU
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